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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,051	03/05/2002	Gerardus Arnoldus Antonius Bos	NL 010979	6456

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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,051	BOS ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-21* is/are rejected.

7)☒ Claim(s) *16-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/4/2005 has been entered.

This is a Non-FINAL Office Action in response to the RCE and AMENDMENT filed 10/4/2005. Claims 1-15 are cancelled. Claims 16-21 are new and under examination.

Response to Amendment

> The specification (including the abstract and claims), and any amendments for applications, except as provided for in 37 CFR 1.821 through 1.825, must have text written plainly and legibly either by a typewriter or machine printer in a nonscript type font (e.g., Arial, Times Roman, or Courier, preferably a font size of 12) lettering style having capital letters which should be at least 0.3175 cm. (0.125 inch) high, but may be no smaller than 0.21 cm. (0.08 inch) high (e.g., a font size of 6) in portrait orientation and presented in a form having sufficient clarity and contrast between the paper and the writing thereon to permit the direct reproduction of readily legible copies in any number by use of photographic, electrostatic, photo-offset, and microfilming processes and electronic capture by use of digital imaging and optical character recognition; and only a single column of text. See 37 CFR 1.52(a) and (b).

The application papers are objected to because the Amendment lacks proper font size. A legible substitute Amendment in compliance with 37 CFR 1.52(a) and (b) and 1.125 is required.

Claim Objections

Claims 16-21 are objected to because of the following informalities:

The reference characters enclosed in parenthesis should be deleted from the claims because they do not have patentable weight. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 16, 19, 20 and 21 recite the expression "at least partially simultaneous", which renders the claim indefinite, because communication of serial or parallel data in a register cannot occur "partially simultaneous" due to the shift timing requirement. During a serial shift function, the clock shifts the data sequentially where the time duration depends on the number of the clock shift pulses, while in a parallel function, the data is clocked "simultaneous".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel (U.S. Patent No. 6,242,269) in view of Nayak (US Patent No. 6,430,718).

Regarding independent Claim 16, as amended, Whetsel discloses a method for testing a testable electronic device (integrated circuit, 700), FIG. 8, having a first plurality of test arrangements (824-842) and a second plurality of test arrangements (924-942), a first shift register (800) forming a data input amplification circuit connected between bond pad 802 and data inputs 804 through 822 to ten plural scan paths 824 through 842, and a second shift register (900) forming a data input amplification circuit connected between terminal 902 and data inputs 904 through 922 to ten plural scan paths 924 through 942, comprising:

Serially communicating first test data (serial test data input from a peripheral bond pad 802) between a first shift register (800) and a first test data channel (802), serially communicating second test data (serial test data input from a peripheral bond pad, 902) between a second shift register (900) and a second test data channel (902).

Parallel communicating through parallel inputs (804-822) the first test data (802) between the first plurality of test arrangements (824-842) and the first shift register (800), and also, parallel communicating through parallel inputs (904-922) the second test data (902) between the second plurality of test arrangements (924-942) and the second shift register (900).

Whetsel does not explicitly disclose that each cell of the first and the second shift register, respectively, is coupled between an external pin and one of the test arrangements.

However, in analogous art, Nayak (US Patent No. 6,430,718) discloses a method of testing integrated circuit, in compliant with IEEE Std 1149.1, including boundary scan cells 24 and 26, which are coupled with input/output pins 18 and 20 and scan elements (SEs) 25 arranged internal to the circuit 14, (Figure 1, Nayak). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the test architecture in the testing method of Whetsel, as taught by Nayak, by sending test vectors in parallel or serial form to input pins of the integrated circuit. A person skilled in the art would have been motivated to do so, since parallel delivery and receipt of test vectors and test results to and from the boundary scan cells provides for ease by which the test vectors can be placed upon the scan elements arranged in one or more chains internal to the core logic. Parallel delivery and receipt greatly enhances the overall test time and minimizes the test vector memory access times of the ATE, see Summary of the Invention, Nayak.

Regarding Claim 17, copying the first test data from the first shift register (800) into a first buffer register (844) through parallel scan paths 1-10 (824-842), and copying the second test data from a second shift register (900) into a second buffer register (944) through parallel scan paths 1-10 (924-942).

Regarding Claim 18, Whetsel discloses method steps of:

Serially communicating the first test data channel (802) to the first shift register (800;

Serially communicating the second test data channel (902) to the second shift register (900).

Parallel communicating the first test data (802) from the first shift register (800) to the first plurality of test arrangements (824-842).

Parallel communicating the second test data (1902) from the second shift register (900) to the second plurality of test arrangements (924-942).

Regarding Claim 19, Whetsel discloses method steps of:

Parallel receiving first test result data (846-864) from the first plurality of test arrangements (824-842) in a third shift register (844).

Parallel receiving second test result data (946-964) from the second plurality of test arrangements (924-942) in a fourth shift register (944).

Serially submitting the first test result data from the third shift register (844) to a third test data channel (866).

Serially submitting the second test result data from the fourth shift register (944) to a fourth test data channel (966).

Regarding independent Claim 20, as amended, Whetsel discloses a testable electronic device (integrated circuit, 700), Figure 8, a first shift register (800) forming a data input amplification circuit connected between bond pad 802 and data inputs 804 through 822 to ten plural scan paths 824 through 842, and a second shift register (900)

forming a data input amplification circuit connected between terminal 902 and data inputs 904 through 922 to ten plural scan paths 924 through 942, comprising:

A first plurality of test arrangements (824-842) and a second plurality of test arrangements (924-942), such as parallel scan paths.

A first contact (802) and a second contact (902), such as bond pads.

A first shift register (800), such as scan distributor coupled between the first contact (802) and the first plurality of test arrangements (824-842) for serially communicating first test data (serial test data input from a peripheral bond pad) with the first contact (802), and for parallel communicating the first test data through parallel inputs (804-822) with the first plurality of test arrangements (824-842) and

A second shift register (900), such as scan distributor coupled between the second contact (902) and the second plurality of test arrangements (924-942) for serially communicating second test data (serial test data input from a peripheral bond pad) with the second contact (902) at least partially simultaneous with the serial communication of the first test data, and for parallel communicating the second test data through parallel inputs (904-922) with the second plurality of test arrangements (924-942) at least partially simultaneous with the parallel communication of the first test data.

A testable electronic device (700, Figure 8), including a first shift register (800) coupled to a first buffer register (844) through parallel scan paths 1-10 (824-842), and a second shift register (900) coupled to a second buffer register (944) through parallel scan paths 1-10 (924-942).

Whetsel does not explicitly disclose that each cell of the first and the second shift register, respectively, is coupled between an external pin and one of the test arrangements.

However, in analogous art, Nayak (US Patent No. 6,430,718) discloses a method of testing integrated circuit, in compliant with IEEE Std 1149.1, boundary scan cells 24 and 26, which are coupled with input/output pins 18 and 20 and scan elements (SEs) 25 arranged internal to the circuit 14, (Figure 1, Nayak). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the test architecture in the testing method of Whetsel, as taught by Nayak, by sending test vectors in parallel or serial form to input pins of the integrated circuit. A person skilled in the art would have been motivated to do so, since parallel delivery and receipt of test vectors and test results to and from the boundary scan cells provides for ease by which the test vectors can be placed upon the scan elements arranged in one or more chains internal to the core logic. Parallel delivery and receipt greatly enhances the overall test time and minimizes the test vector memory access times of the ATE, see Summary of the Invention, Nayak.

Regarding Claim 21, Whetsel discloses a testable electronic device (700), wherein the first shift register (800) is arranged to communicate the first test data from the first contact (802) to the first plurality of test arrangements (824-842), and the second shift register (900) is arranged to communicate the second test data from the second contact (902) to the second plurality of test arrangements (924-942), and wherein the electronic device (700) further comprises:

A third contact (866) and a fourth contact (966);

A third shift register (844) coupled between the third contact (866) and the first plurality of test arrangements (824-842) for serially submitting first test result data to the third contact (206), and for parallel receiving the first test result data (846-864) from the first plurality of test arrangements (824-842).

A fourth shift register (944) coupled between the fourth contact (966) and the second plurality of test arrangements (924-942) for serially submitting second test result data to the fourth contact (966) at least partially simultaneous with the serial submission of the first test result data, and for parallel receiving the second test result data (946-964) from the second plurality of test arrangements (924-942) at least partially simultaneous with the parallel reception of the first test result data.

Response to Arguments

Applicant's arguments filed 10/4/2005 with respect to claims 16-21 have been considered but are moot in view of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

By: _____.

Randolph Building, 401 Dulany Street,
Alexandria, VA 22314
Tel: (571) 272-3824, Fax: (571) 273-3824
james.kerveros@uspto.gov

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Office Action: Non-Final Rejection